TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS044

CD4047B Types

CMOS Low-Power Monostable/Astable Multivibrator

High Voltage Types (20-Volt Rating)

■ CD4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are $\overline{Q}$, Q, and OSCILLATOR. In all modes of operation, and external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the $\overline{\text{ASTABLE}}$ input, or both. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047B triggers in the monostable mode when a positive-going edge occurs on the +TRIGGER-input while the -TRIGGER is held low. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive-going edge. The CD4047B will retrigger as long as the RETRIGGER-input is high, with or without transitions (See Fig. 34).

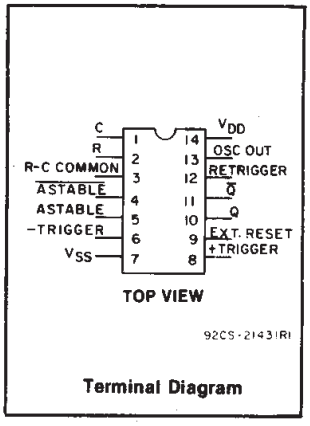
An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. For monostable operation, whenever V_{DD} is applied, an internal power-on reset circuit will clock the Q output low within one output period (t_M).

The CD4047B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- *Low power consumption: special CMOS oscillator configuration*
- *Monostable (one-shot) or astable (free-running) operation*
- *True and complemented buffered outputs*
- *Only one external R and C required*
- *Buffered inputs*
- *100% tested for quiescent current at 20 V*
- *Standardized, symmetrical output characteristics*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*



Terminal Diagram

Monostable Multivibrator Features:

- *Positive- or negative-edge trigger*
- *Output pulse width independent of trigger pulse duration*
- *Retriggerable option for pulse width expansion*
- *Internal power-on reset circuit*
- *Long pulse widths possible using small RC components by means of external counter provision*
- *Fast recovery time essentially independent of pulse width*
- *Pulse-width accuracy maintained at duty cycles approaching 100%*

Astable Multivibrator Features:

- *Free-running or gatable operating modes*
- *50% duty cycle*
- *Oscillator output available*
- *Good astable frequency stability:*
  Frequency deviation:
  = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ±10%)

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- *Envelope detection*
- *Frequency multiplication*
- *Frequency division*
- *Frequency discriminators*
- *Timing circuits*
- *Time-delay applications*

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V
NOTE: IF AT 15 V OPERATION A 10 MΩ RESISTOR IS USED THE OPERATING TEMPERATURE SHOULD BE BETWEEN −25°C and 100°C			

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

CD4047B FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	—	10,11,13	t_A (10,11) = 4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A (13) = 2.20 RC#
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	t_M (10,11) = 2.48 RC
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	—	10,11	

▲ See Text.

First positive ½ cycle pulse-width = 2.48 RC, see Note on Page 3-134.

* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4

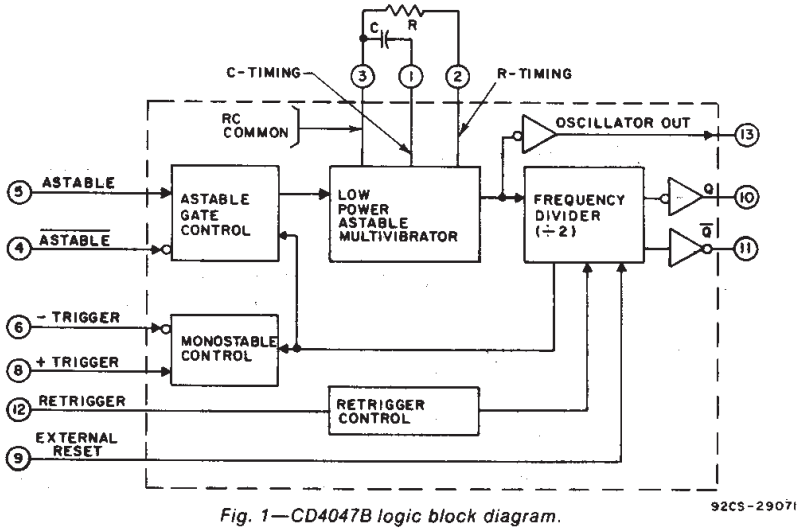


Fig. 1—CD4047B logic block diagram.

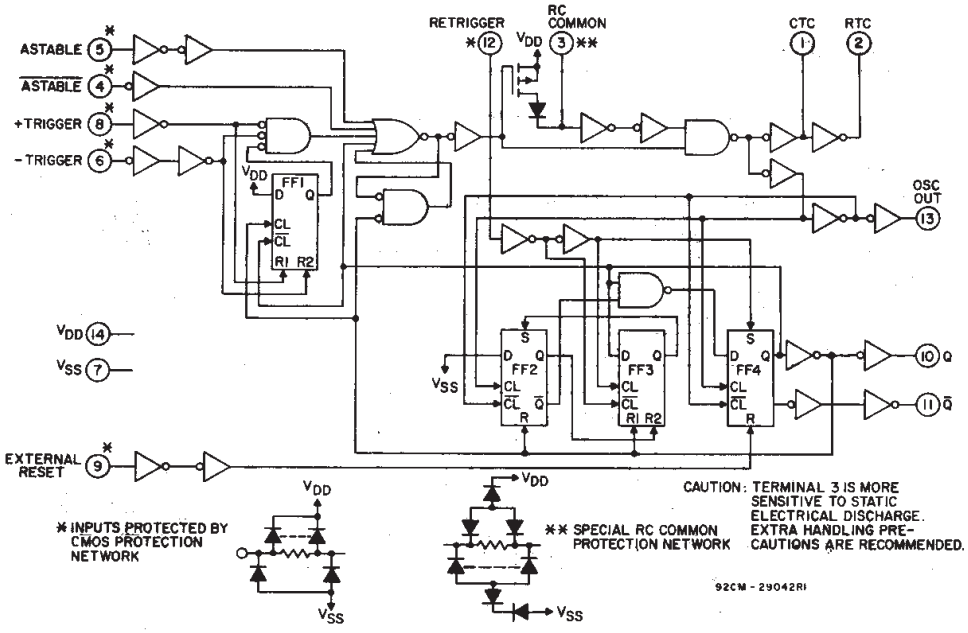


Fig. 2—CD4047B logic diagram.

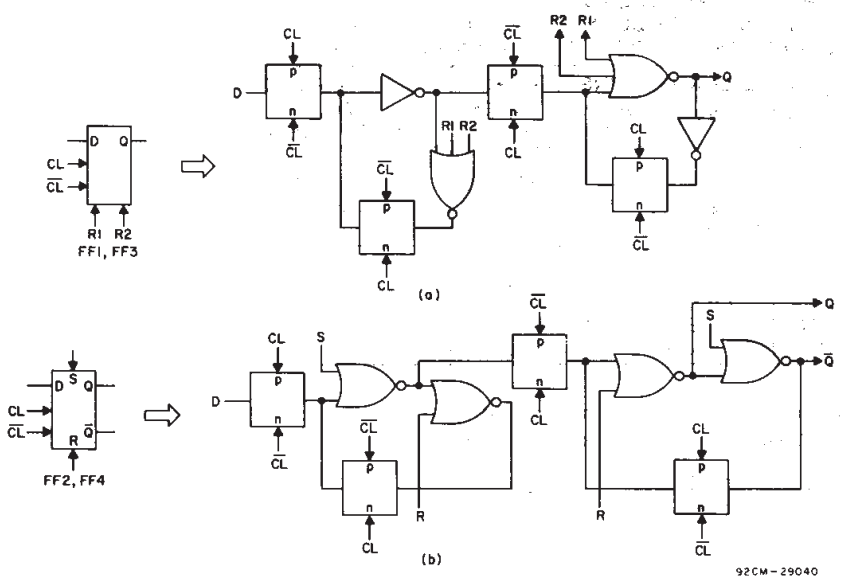


Fig. 3—Detail logic diagram for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b).

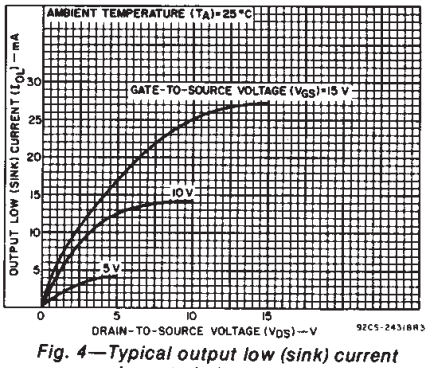


Fig. 4—Typical output low (sink) current characteristics.

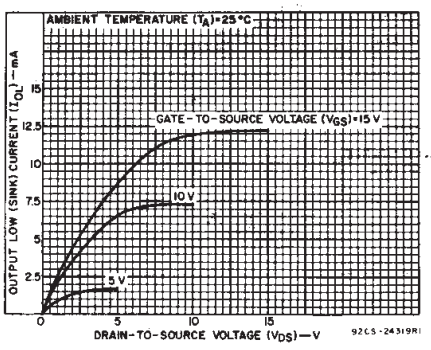


Fig. 5—Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	

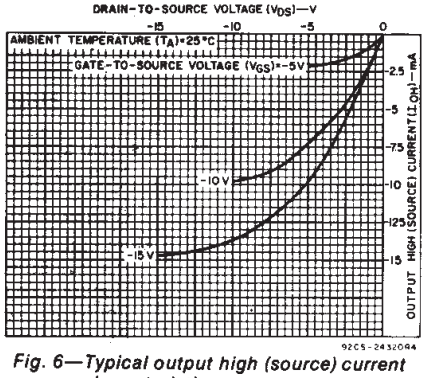


Fig. 6—Typical output high (source) current characteristics.

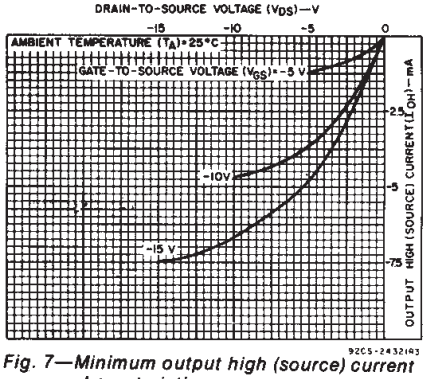


Fig. 7—Minimum output high (source) current characteristics.

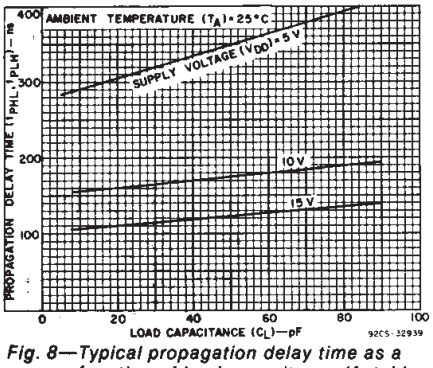


Fig. 8—Typical propagation delay time as a function of load capacitance (Astable, Astable to Q, $\overline{Q}$).

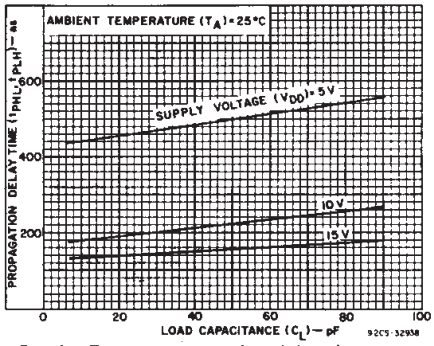


Fig. 9—Typical propagation delay time as a function of load capacitance (+ or − trigger to Q, $\overline{Q}$).

STATIC ELECTRICAL CHARACTERISTICS (CONTINUED)

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1.9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10^5	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}					
Astable, $\overline{\text{Astable}}$ to Osc. Out	5	—	200	400	ns
	10	—	100	200	
	15	—	80	160	
Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	5	—	350	700	
	10	—	175	350	
	15	—	125	250	
+ or − Trigger to Q, $\overline{Q}$	5	—	500	1000	
	10	—	225	450	
	15	—	150	300	
Retrigger to Q, $\overline{Q}$	5	—	300	600	
	10	—	150	300	
	15	—	100	200	
External Reset to Q, $\overline{Q}$	5	—	250	500	
	10	—	100	200	
	15	—	70	140	
Transition Time, t_{THL}, t_{TLH} Osc. Out, Q, $\overline{Q}$	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Input Pulse Width, t_W	5	—	200	400	
+ Trigger, − Trigger	10	—	80	160	
	15	—	50	100	
Reset	5	—	100	200	
	10	—	50	100	
	15	—	30	60	
Retrigger	5	—	300	600	
	10	—	115	230	
	15	—	75	150	
Input Rise and Fall Time, t_r, t_f All Trigger Inputs					
For + Trigger: t_f	5	—	270	—	
t_r only is unlimited	10	—	18	—	
	15	—	9	—	μs
For − Trigger: t_r	5	—	325	—	
t_f only is unlimited	10	—	9	—	
	15	—	4	—	
Q or $\overline{Q}$ Deviation from 50% Duty Factor	5	—	±0.5	±1	
	10	—	±0.5	±1	%
	15	—	±0.1	±0.5	
Input Capacitance, C_{IN}	Any Input	—	5	7.7	pF

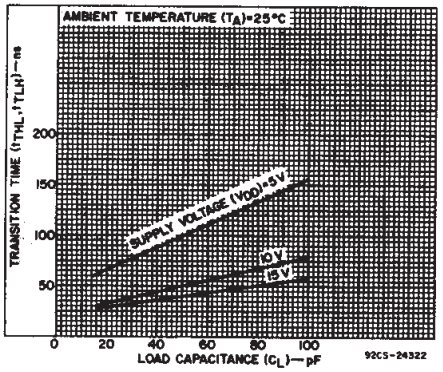


Fig. 10—Typical transition time as a function of load capacitance.

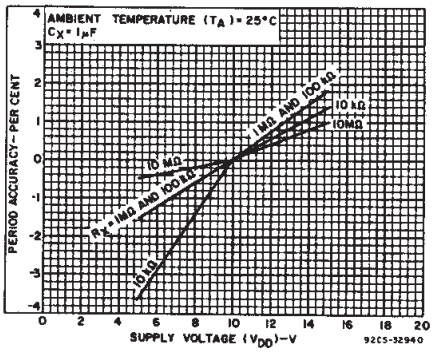


Fig. 11—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

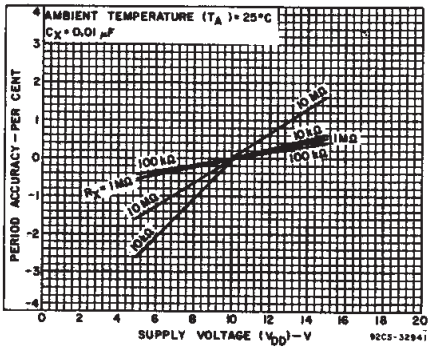


Fig. 12—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

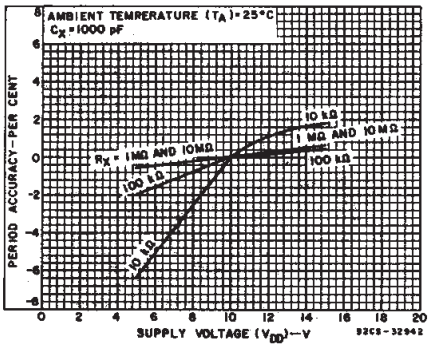


Fig. 13—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

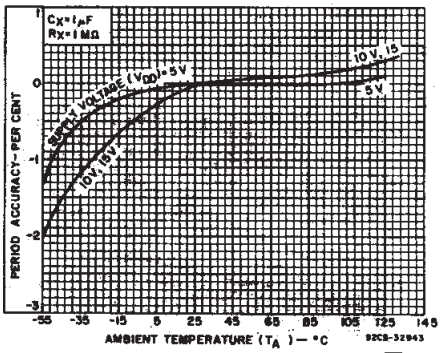


Fig. 14—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (ultra-low frequency).

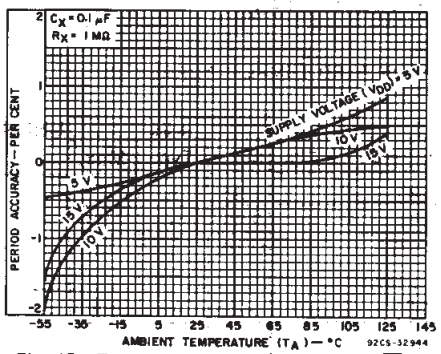


Fig. 15—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (low frequency).

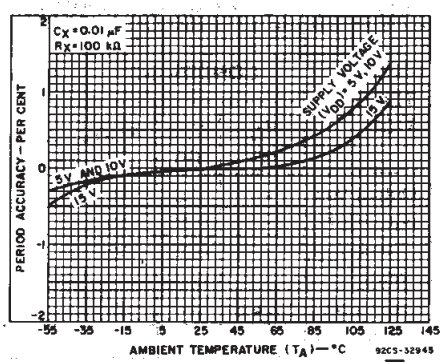


Fig. 16—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (medium frequency).

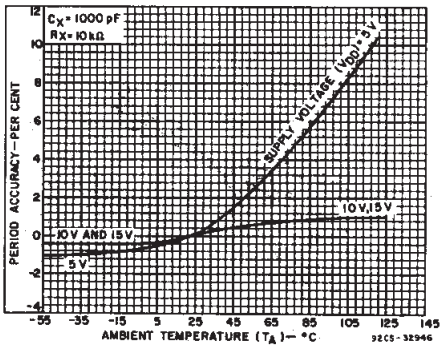


Fig. 17—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (high-frequency).

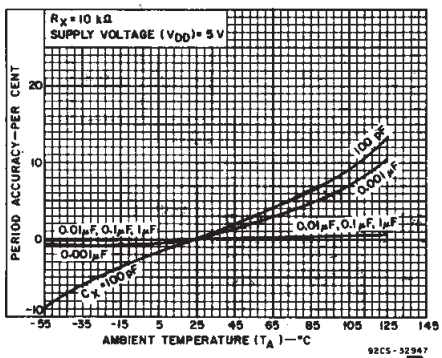


Fig. 18—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature.

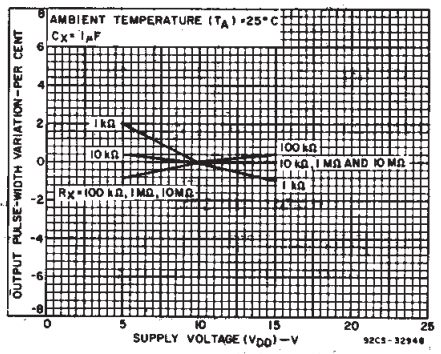


Fig. 19—Typical output pulse-width variations vs. supply voltage.

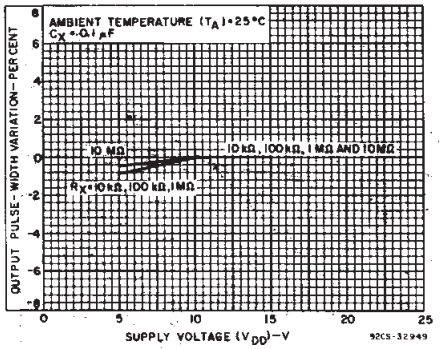


Fig. 20—Typical output pulse-width variations vs. supply voltage.

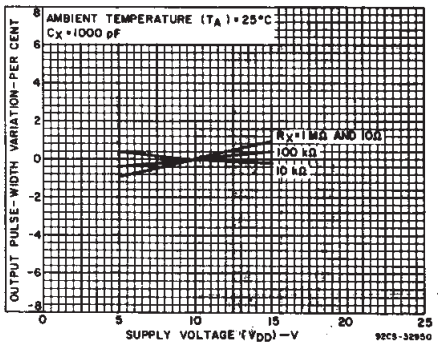


Fig. 21—Typical output pulse-width variations vs. supply voltage.

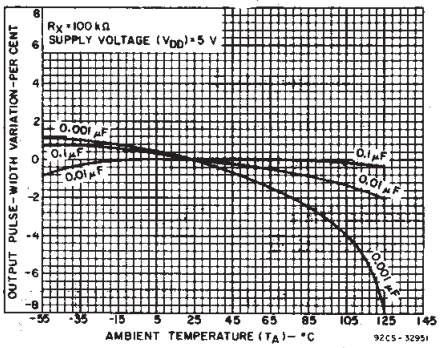


Fig. 22—Typical output pulse-width variations vs. ambient temperature.

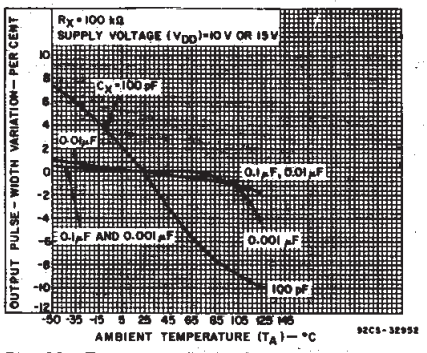


Fig. 23—Typical output pulse-width variations vs. ambient temperature.

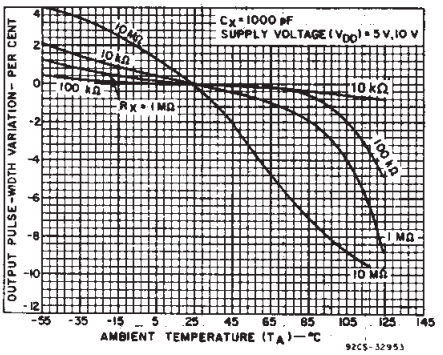


Fig. 24—Typical output-pulse-width variations vs. ambient temperature.

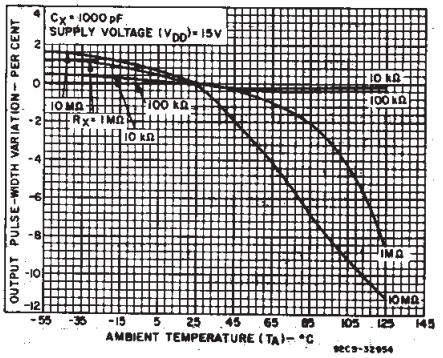


Fig. 25—Typical output pulse-width variations vs. ambient temperature.

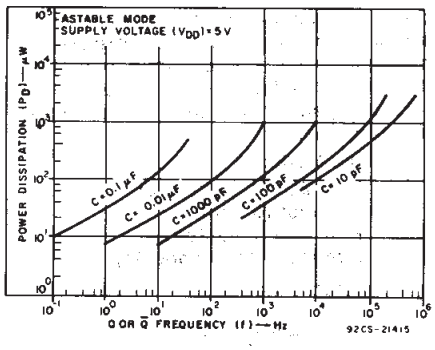


Fig. 26—Typical power dissipation vs. output frequency (V_{DD} = 5 V).

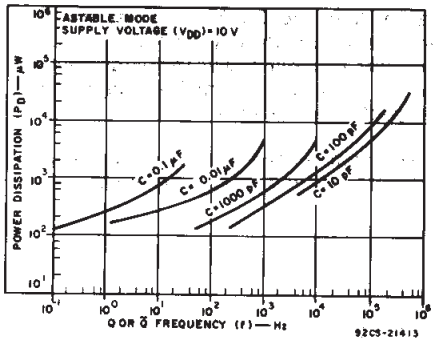


Fig. 27—Typical power dissipation vs. output frequency (V_{DD} = 10 V).

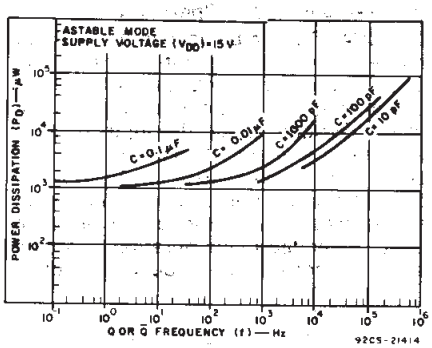


Fig. 28—Typical power dissipation vs. output frequency (V_{DD} = 15 V).

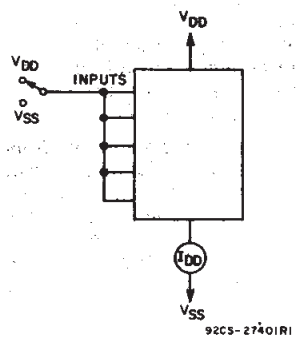


Fig. 29—Quiescent device current test circuit.

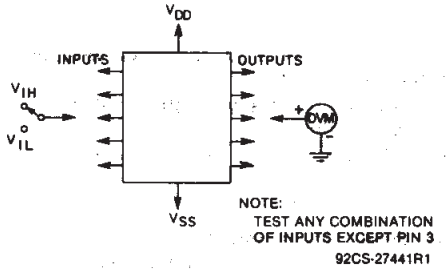


Fig. 30—Input-voltage test circuit.

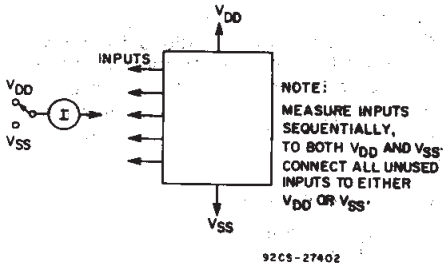


Fig. 31—Input-leakage-current test circuit.

1. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations — The following analysis presents variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for free-running (astable) operation.

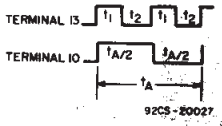


Fig. 32—Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}};$$

typically, $t_1 = 1.1\ RC$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}};$$

typically, $t_2 = 1.1\ RC$

$$t_A = 2(t_1 + t_2)$$

$$= -2\ RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$

thus if $t_A = 4.40\ RC$ is used, the variation will be +5%, −0% due to variations in transfer voltage.

B. Variations Due to V_{DD} and Temperature Changes — In addition to variations from unit to unit, the astable period varies with V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 11 to 18 with 10 V as reference for voltage variations curves and 25°C as reference for temperature variations curves.

II. Monostable Mode Design Information

The following analysis presents variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% — 67% V_{DD}) for one-shot (monostable) operation.

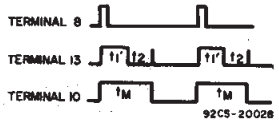


Fig. 33—Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

typically, $t_1' = 1.38\ RC$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

thus if $t_M = 2.48\ RC$ is used, the variation will be +9.3%, −0% due to variations in transfer voltage.

Note:

In the astable mode, the first positive half cycle has a duration of t_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width varies with V_{DD} and temperature. These variations are presented in graphical form in Fig. 19 to 26 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

III. Retrigger Mode Operation

The CD4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminal 12, and the output is taken from terminal 10 or 11. As shown in Fig. 34 normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied.

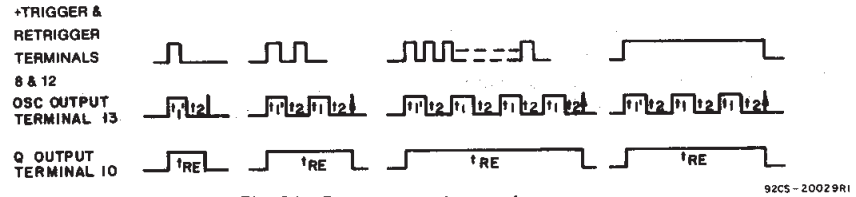


Fig. 34—Retrigger-mode waveforms.

For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, the output pulse width is an integral number of time periods, with the first time period being $t_1' + t_2$, typically, 2.48RC, and all subsequent time periods being $t_1 + t_2$, typically, 2.2RC.

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 35. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

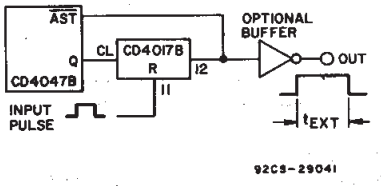


Fig. 35—Implementation of external counter option.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be at least an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$ pF, up to any practical value, for astable modes;

$C \geq 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leq R \leq 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode:

$P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

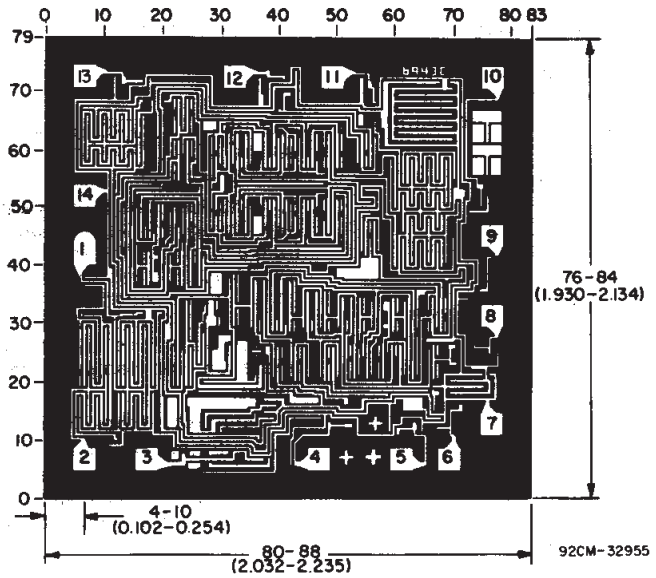
Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 27, 28, and 29 for typical power consumption in astable mode.



Chip dimensions and pad layout for CD4047B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.